Claims

[c1] 1. A polysilicon thin film transistor, comprising:
a substrate;
a poly-island layer over the substrate, wherein the poly-island layer having:
a channel region, and
a doped source/drain region on each side of the channel region;
a gate over the channel region of the poly-island layer;
a gate insulating film between the gate and the poly-island layer, the gate insulating film further comprising:
a silicon oxide layer covering the poly-island layer; and
a silicon nitride layer between the silicon oxide layer and the gate; and
an inter-layer dielectric over the gate and the gate insulating film.

[c2] 2. The polysilicon thin film transistor of claim 1, wherein the silicon oxide has a thickness between about 100Å to 1400Å.

[c3] 3. The polysilicon thin film transistor of claim 1, wherein the silicon nitride layer has a thickness between about 50Å to 400Å.

[c4] 4. The polysilicon thin film transistor of claim 1, wherein the doped source/drain region includes an N-doped region.

[c5] 5. The polysilicon thin film transistor of claim 1, wherein the doped source/drain region includes a P-doped region.

[c6] 6. The polysilicon thin film transistor of claim 5, wherein the poly-island layer may further include a lightly doped drain region between the channel region and the doped source/drain region.

[c7] 7. The polysilicon thin film transistor of claim 1, wherein the transistor may further include a buffer layer directly formed over the substrate.

[c8] 8. A polysilicon thin film transistor, comprising:
a gate;
a poly-island layer under the gate, wherein the poly-island layer further includes a channel region under the gate and a doped source/drain region on each side of the channel region;
a gate insulating film between the gate and the poly-island layer, wherein the gate insulating film includes a silicon oxide layer and a silicon nitride layer, wherein the silicon oxide layer covers the poly-island layer; and

the silicon nitride layer is between the silicon oxide layer and the gate;

a first inter-layer dielectric over the gate and the gate insulating film;

a source/drain contact metal embedded between the first inter-layer dielectric and the gate insulating film on each side of the gate, wherein the source/drain contact metal is electrically connected to the doped source/drain region; and

a second inter-layer dielectric covering the first inter-layer dielectric and the source/drain contact metal.

[c9] 9. The polysilicon thin film transistor of claim 8, wherein the silicon oxide has a thickness between about 100Å to 1400Å.

[c10] 10. The polysilicon thin film transistor of claim 8, wherein the silicon nitride layer has a thickness between about 50Å to 400Å.

[c11] 11. The polysilicon thin film transistor of claim 8, wherein the doped source/drain region includes an N-doped region.

[c12] 12. The polysilicon thin film transistor of claim 8, wherein the doped source/drain region includes a P-doped region.

[c13] 13. The polysilicon thin film transistor of claim 12, wherein the poly-island layer may further include a lightly doped drain region between the channel region and the doped source/drain region.

[c14] 14. The polysilicon thin film transistor of claim 8, wherein the transistor may further include a buffer layer directly formed over the substrate.